

OCM128128-2 图形点阵液晶显示模块

使用说明书

感谢您关注和使用我们的液晶显示器产品， 欢迎您提出您的要求、意见和建议，我们将竭诚为您服务、让您满意。您可以浏览 www.GPTLCM.CN 了解最新的产品与应用信息,或拨打热线电话 0758-2317156 以及向 syl@gptlcm.cn 邮箱发 E-mail 获取具体的技术咨询与服务

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初始化程序参考

模块外形图

1、 产品简介

主要工艺: COG
显示内容: 128X128 点阵
显示模式: STN, POSITIVE
驱动条件: 1/128Duty,1/9Bias
视向: 6: 00
背光: LED, 白色
工作温度: -20℃ -+70℃
储存温度: -30℃ -+80℃
驱动 IC: ST7541_14

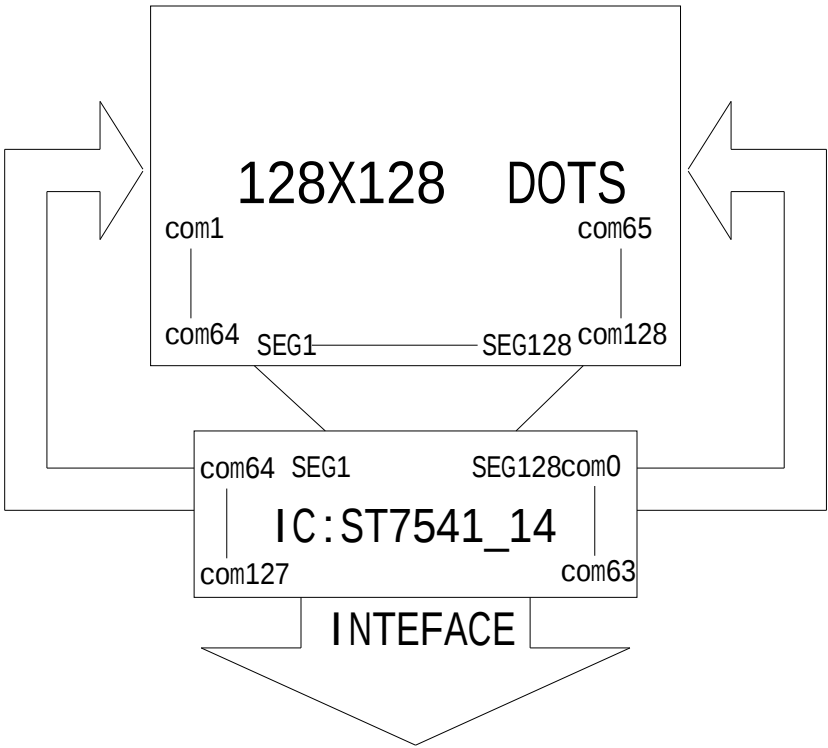
2、 引用文件

ST7541_14 规格书

3、 机械特性

类别	标准值	单位
模块	65.0（w）X66.5(h)X7.0(t)Max	mm
有效显示区	48.78(w)X48.78(h)	mm
点大小	0.33(w)X0.33(h)	mm
点间隙	0.02(w)X0.02(h)	mm

4、 产品框图



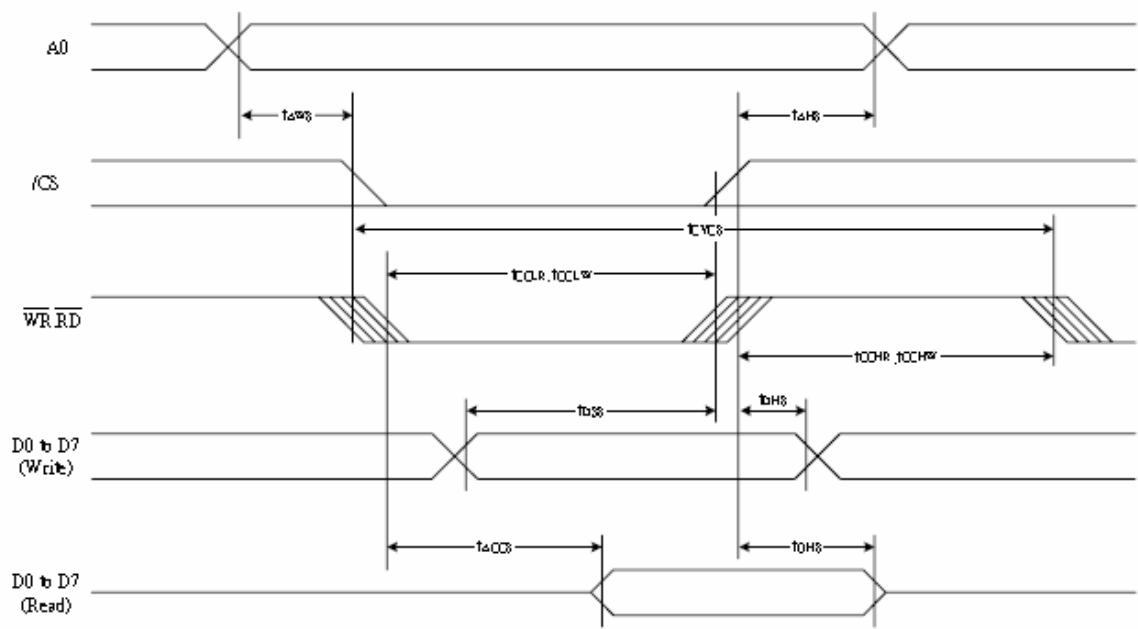
5、光电特性

类别	符号	条件	最小值	TYP	最大值	单位
驱动电压	Vop.	25℃	8.8	9.0	9.2	V
响应时间	Ton	25℃	—	127	400	Ms
对比度	Toff	25℃	—	263	400	Ms
	CR	25℃	—	9	—	—
视角范围		25℃	—	88	—	DEG
交叉效应		25℃	—	1.2	—	—

6、极限参数

参数	符号	最小值	最大值	单位
逻辑电压	Vdd	-0.3	+3.3	V
驱动电压	Vout,VO	-0.3	+17.0	V
工作温度	Top	-10	+60	℃
存储温度	Tst	-20	+70	℃

7、接口时序



(VDD = 3.3V, Ta = 25°C)

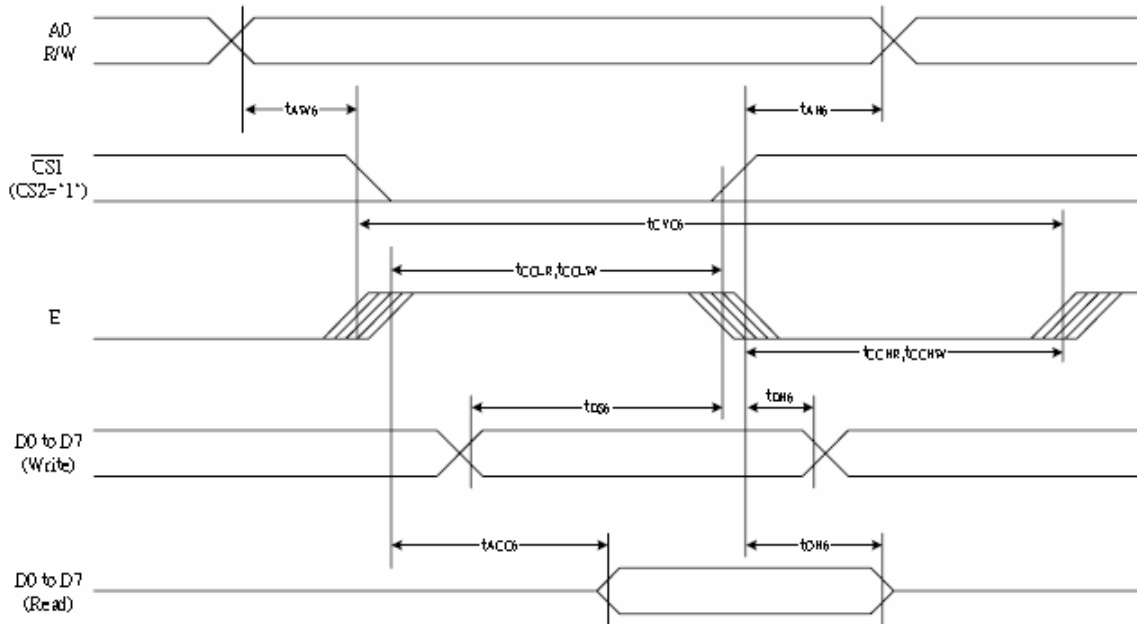
Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH8		0	—	ns
Address setup time		tAW8		0	—	
System cycle time		tCYC8		240	—	
Enable L pulse width (WRITE)	WR	tCCLW		80	—	
Enable H pulse width (WRITE)		tCCHW		80	—	
Enable L pulse width (READ)	RD	tCCLR		140	—	
Enable H pulse width (READ)		tCCHR		80	—	
WRITE Data setup time	D0 to D7	tDS8		40	—	
WRITE Data hold time		tDH8		10	—	
READ access time		tACC8	CL = 100 pF	—	70	
READ Output disable time		tOH8	CL = 100 pF	5	50	

(VDD = 2.7 V, Ta = 25°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH8		0	—	ns
Address setup time		tAW8		0	—	
System cycle time		tCYC8		400	—	
Enable L pulse width (WRITE)	WR	tCCLW		220	—	
Enable H pulse width (WRITE)		tCCHW		180	—	
Enable L pulse width (READ)	RD	tCCLR		220	—	
Enable H pulse width (READ)		tCCHR		180	—	
WRITE Data setup time	D0 to D7	tDS8		40	—	
WRITE Data hold time		tDH8		15	—	
READ access time		tACC8	CL = 100 pF	—	140	
READ Output disable time		tOH8	CL = 100 pF	10	100	

(VDD = 1.8V, Ta = 25°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH8		0	—	ns
Address setup time		tAW8		0	—	
System cycle time		tCYC8		640	—	
Enable L pulse width (WRITE)	WR	tCCLW		360	—	
Enable H pulse width (WRITE)		tCCHW		280	—	
Enable L pulse width (READ)	RD	tCCLR		360	—	
Enable H pulse width (READ)		tCCHR		280	—	
WRITE Data setup time	D0 to D7	tDS8		80	—	
WRITE Data hold time		tDH8		30	—	
READ access time		tACC8	CL = 100 pF	—	240	
READ Output disable time		tOH8	CL = 100 pF	10	200	



(VDD = 3.3 V, Ta = 25°C)

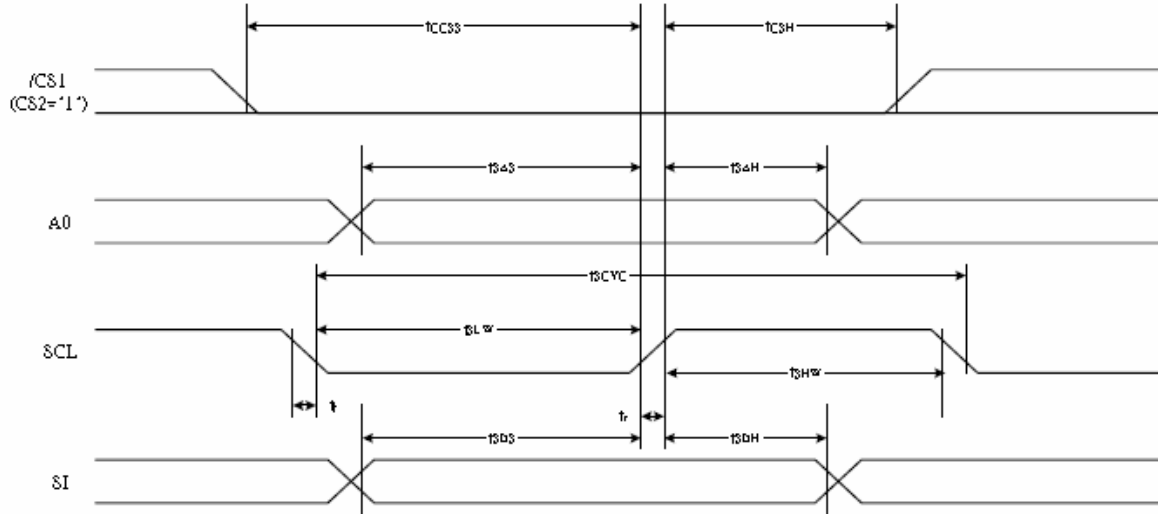
Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH6		0	—	ns
Address setup time		tAW6		0	—	
System cycle time		tCYC6		240	—	
Enable L pulse width (WRITE)	WR	tEWLW		80	—	
Enable H pulse width (WRITE)		tEWHW		80	—	
Enable L pulse width (READ)	RD	tEWLR		80	—	
Enable H pulse width (READ)		tEWHR		140	—	
WRITE Data setup time	D0 to D7	tDS6		40	—	
WRITE Data hold time		tDH6		10	—	
READ access time		tACC6	CL = 100 pF	—	70	
READ Output disable time		tOH6	CL = 100 pF	5	50	

(VDD = 2.7V, Ta = 25°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH6		0	—	ns
Address setup time		tAW6		0	—	
System cycle time		tCYC6		400	—	
Enable L pulse width (WRITE)	WR	tEWLW		220	—	
Enable H pulse width (WRITE)		tEWHW		180	—	
Enable L pulse width (READ)	RD	tEWLR		220	—	
Enable H pulse width (READ)		tEWHR		180	—	
WRITE Data setup time	D0 to D7	tDS6		40	—	
WRITE Data hold time		tDH6		15	—	
READ access time		tACC6	CL = 100 pF	—	140	
READ Output disable time		tOH6	CL = 100 pF	10	100	

(VDD=1.8V, Ta=25°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH6		0	—	ns
Address setup time		tAW6		0	—	
System cycle time		tCYC6		640	—	
Enable L pulse width (WRITE)	WR	tEWLW		360	—	
Enable H pulse width (WRITE)		tEWHW		280	—	
Enable L pulse width (READ)	RD	tEWLR		360	—	
Enable H pulse width (READ)		tEWHR		280	—	
WRITE Data setup time	D0 to D7	tDS6		80	—	
WRITE Data hold time		tDH6		30	—	
READ access time		tACC6	CL = 100 pF	—	240	
READ Output disable time		tOH6	CL = 100 pF	10	200	



(VDD=3.3V, Ta=25°C)

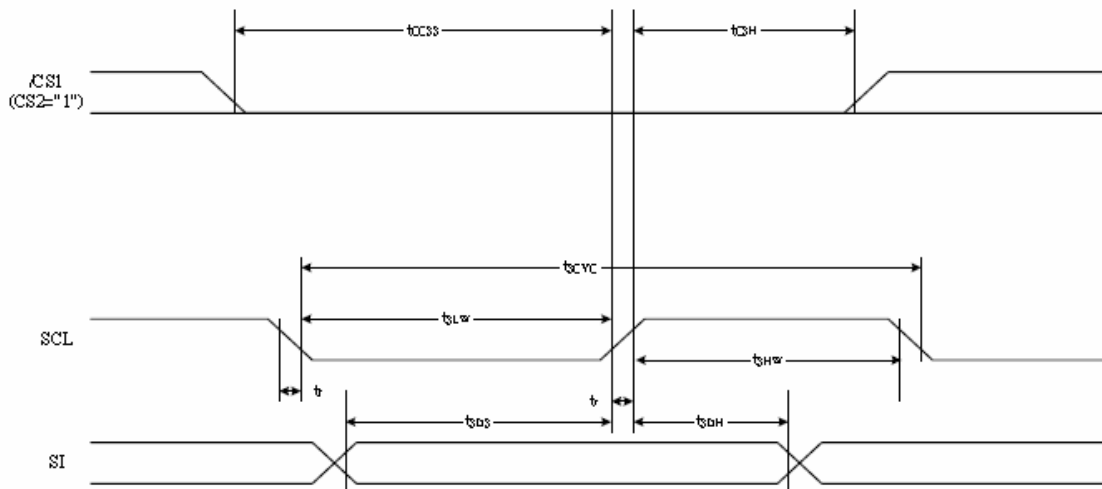
Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	tSCYC		50	—	ns
SCL "H" pulse width		tSHW		25	—	
SCL "L" pulse width		tSLW		25	—	
Address setup time	A0	tSAS		20	—	
Address hold time		tSAH		10	—	
Data setup time	SI	tSDS		20	—	
Data hold time		tSDH		10	—	
CS-SCL time	CSB	tCSS		20	—	
CS-SCL time		tCSH		40	—	

(V_{DD}=2.7V, Ta=25°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	tSCYC		100	—	ns
SCL "H" pulse width		tSHW		50	—	
SCL "L" pulse width		tSLW		50	—	
Address setup time	A0	tSAS		30	—	
Address hold time		tSAH		20	—	
Data setup time	SI	tSDS		30	—	
Data hold time		tSDH		20	—	
CS-SCL time	CSB	tCSS		30	—	
CS-SCL time		tCSH		60	—	

(V_{DD}=1.8V, Ta=25°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	tSCYC		200	—	ns
SCL "H" pulse width		tSHW		80	—	
SCL "L" pulse width		tSLW		80	—	
Address setup time	A0	tSAS		60	—	
Address hold time		tSAH		30	—	
Data setup time	SI	tSDS		60	—	
Data hold time		tSDH		30	—	
CS-SCL time	CSB	tCSS		40	—	
CS-SCL time		tCSH		100	—	

SERIAL INTERFACE (3-Line Interface)

(V_{DD}=3.3V, T_a=25°C)

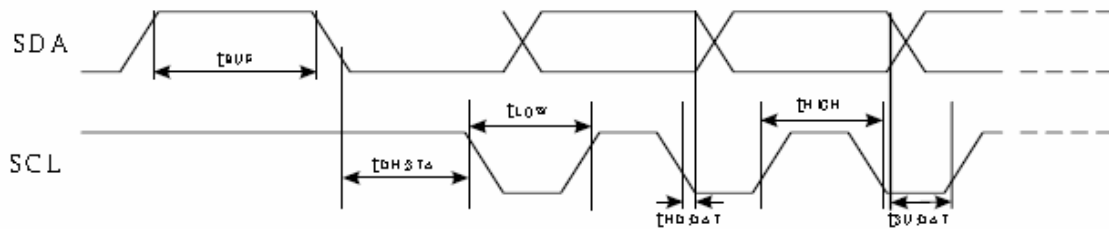
Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	tSCYC		50	—	ns
SCL "H" pulse width		tSHW		25	—	
SCL "L" pulse width		tSLW		25	—	
Data setup time	SI	tSDS		20	—	
Data hold time		tSDH		10	—	
CS-SCL time	CSB	tCSS		20	—	
CS-SCL time		tCSH		40	—	

(V_{DD}=2.7V, T_a=25°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	tSCYC		100	—	ns
SCL "H" pulse width		tSHW		50	—	
SCL "L" pulse width		tSLW		50	—	
Data setup time	SI	tSDS		30	—	
Data hold time		tSDH		20	—	
CS-SCL time	CSB	tCSS		30	—	
CS-SCL time		tCSH		60	—	

(V_{DD}=1.8V, T_a=25°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	tSCYC		200	—	ns
SCL "H" pulse width		tSHW		80	—	
SCL "L" pulse width		tSLW		80	—	
Data setup time	SI	tSDS		60	—	
Data hold time		tSDH		30	—	
CS-SCL time	CSB	tCSS		40	—	
CS-SCL time		tCSH		100	—	

SERIAL INTERFACE (IIC Interface)

(V_{DD}=3.3V, Ta=25°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
SCL clock frequency	SCL	F _{SCLK}		-	400	KHZ
SCL clock low period	SCL	T _{LOW}		1.3	-	us
SCL clock high period	SCL	T _{HIGH}		0.6	-	us
Data set-up time	SI	T _{SU} ;Data		100	-	ns
Data hold time	SI	T _{HD} ;Data		0	0.9	us
SCL,SDA rise time	SCL	T _R		20+0.1Cb	300	ns
SCL,SDA fall time	SCL	T _F		20+0.1Cb	300	ns
Capacitive load represented by each bus line		C _b		-	400	pF
Setup time for a repeated START condition	SI	T _{SU} ;SUA		0.6	-	us
Start condition hold time	SI	T _{HD} ;STA		0.6	-	us
Setup time for STOP ondition		T _{SU} ;STO		0.6	-	us
Tolerable spike width on bus		T _{SW}		-	50	ns
BUS free time between a STOP and START condition	SCL	T _{BUF}		1.3		us

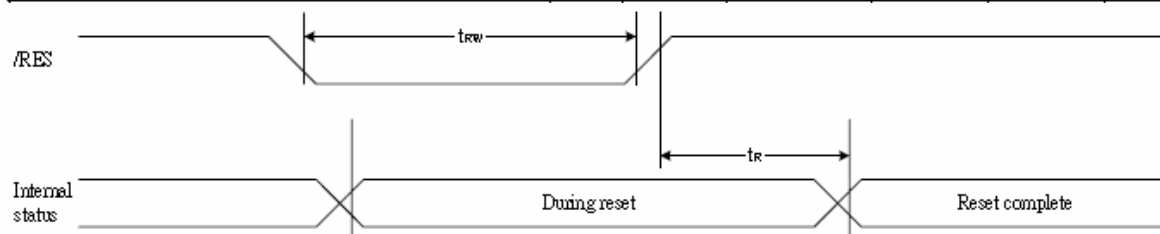


Figure 34

(V_{DD} = 3.3V , Ta = -40 to 85°C)

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time		t _R		—	—	1	us
Reset "L" pulse width	RESB	t _{RW}		1	—	—	us

(V_{DD} = 2.7V , Ta = -40 to 85°C)

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time		t _R		—	—	1.5	us
Reset "L" pulse width	RESB	t _{RW}		1.5	—	—	us

(V_{DD} = 1.8V , Ta = -40 to 85°C)

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time		t _R		—	—	2.0	us
Reset "L" pulse width	RESB	t _{RW}		2.0	—	—	us

8、直流特性 (VDD=2.84V)

$V_{DD} = 1.7\text{ V to } 3.3\text{ V}$; $V_{SS} = 0\text{ V}$; $V_{LCD} = 3.0\text{ to } 13.0\text{ V}$; $T_{amb} = -40^{\circ}\text{C to } +85^{\circ}\text{C}$; unless otherwise specified.

Item		Symbol	Condition		Rating			Units	Applicable Pin
					Min.	Typ.	Max.		
Operating Voltage (1)		VDD1			1.7	—	3.3	V	Vss*1
Operating Voltage (2)		VDD2	(Relative to VSS)		1.7	—	3.3	V	VSS2
High-level Input Voltage		VIHC			0.7 x VDD	—	VDD	V	*2
Low-level Input Voltage		VILC			VSS	—	0.3 x VDD	V	*2
High-level Output Voltage		VOHC			0.7 x VDD	—	VDD	V	*3
Low-level Output Voltage		VOLC			VSS	—	0.3 x VDD	V	*3
Input leakage current		ILI	VIN = VDD or VSS		−1.0	—	1.0	μA	*4
Output leakage current		ILO	VIN = VDD or VSS		−3.0	—	3.0	μA	*5
Liquid Crystal Driver ON Resistance		RON	Ta = 25°C	VOUT_IN = 15.0 V	—	2.0	3.5	KΩ	SEGn COMn *6
			(Relative To VSS)	VOUT_IN = 8.0 V	—	3.2	5.4		
Oscillator Frequency	Internal Oscillator	fOSC	1/128 duty Ta = 25°C 9 PWM		—	443.5	462.5	kHz	*7
	External Input	fCL			—	88.7	92.5	kHz	OSC
	Frame frequency	fFRAME			—	77	85	Hz	

Item	Symbol	Condition	Rating			Units	Applicable Pin
			Min.	Typ.	Max.		
Internal Power	Input voltage	VDD	(Relative To VSS)	1.7	—	3.3	V
	Supply Step-up output voltage Circuit	VOUT_OUT	(Relative To VSS)	—	—	15	V
	Voltage regulator Circuit Operating Voltage	VOUT_IN	(Relative To VSS)	—	—	15	V

9、引脚描述

接口定义:

引脚编号	引脚名称	方向	引脚功能描述
1	VSS	I	逻辑电源地 0V
2	VDD	I	逻辑电源正 3.3V
3	NC (V0)	I	悬空 (LCD 驱动输入)
4	A0	-	数据\指令选择: 高电平: DB0-DB7 为显示数据 低电平: DB0-DB7 为操作指令
5	RW/WR	I	读/写控制脚: 当接口定义为 6800 接口时, RW=H: 读操作 RW=L: 写操作 当接口定义为 8080 接口时, /WR 为写入控制脚
6	E/RD	I/O	当接口定义为 6800 接口时, 为使能控制脚, E=H 有效 当接口定义为 8080 接口时, /RD 为读控制脚, 低有效
7	DB0	I/O	数据输入输出引脚
8	DB1	I/O	数据输入输出引脚
9	DB2	I/O	数据输入输出引脚
10	DB3	I/O	数据输入输出引脚
11	DB4	I/O	数据输入输出引脚
12	DB5	I/O	数据输入输出引脚
13	DB6	I/O	数据输入输出引脚
14	DB7	I	数据输入输出引脚
15	CSB		片选择信号, 低电平时有效
16	PS1	-	接口方式选择: 高电平: 接口定义为 6800 接口 低电平: 接口定义为 8080 接口
17	/RST	0	复位信号, 低电平有效
18	NC (VEE)	0	悬空 (LCD 驱动输出)
19	LED+	I	背光电源, LED+ (3.3V)
20	LED-	I	背光电源, LED- (0V)

10、命令描述

指令表:

Instruction	A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description
Mode Set	0	0	0	0	1	1	1	0	0	0	2-byte instruction to set Mode and FR(Frame frequency control) BE(Booster efficiency control)
	0	0	FR3	FR2	FR1	FR0	0	BE	x'	0	
Read display data	1	1	Read data								Read data into DDRAM
Write display data	1	0	Write data								Write data into DDRAM
Read status	0	1	BUSY	ON	RES	MF2	MF1	MF0	DS1	DS0	Read the internal status
ICON control register ON/OFF	0	0	1	0	1	0	0	0	1	ICON	ICON=0: ICON disable(default) ICON=1: ICON enable & set the page address to 16
Set page address	0	0	1	0	1	1	P3	P2	P1	P0	Set page address
Set column address MSB	0	0	0	0	0	1	0	Y7	Y6	Y5	Set column address MSB
Set column address LSB	0	0	0	0	0	0	Y4	Y3	Y2	Y1	Set column address LSB
Set modify-read	0	0	1	1	1	0	0	0	0	0	Set modify-read mode
Reset modify-read	0	0	1	1	1	0	1	1	1	0	release modify-read mode
Display ON/OFF	0	0	1	0	1	0	1	1	1	D	D=0: Display OFF D=1: Display ON
Set initial display line register	0	0	0	1	0	0	0	0	x'	x'	2-byte instruction to specify the initial display line to realize vertical scrolling
	0	0	x'	S6	S5	S4	S3	S2	S1	S0	
Set initial COM0 register	0	0	0	1	0	0	0	1	x'	x'	2-byte instruction to specify the initial COM0 to realize window scrolling
	0	0	x'	C6	C5	C4	C3	C2	C1	C0	
Set partial display duty ration	0	0	0	1	0	0	1	0	x'	x'	2-byte instruction to set partial display duty ratio
	0	0	D7	D6	D5	D4	D3	D2	D1	D0	
Set N-line inversion	0	0	0	1	0	0	1	1	x'	x'	2-byte instruction to set N-line inversion register
	0	0	x'	x'	x'	N4	N3	N2	N1	N0	
Release N-line inversion	0	0	1	1	1	0	0	1	0	0	Release N-line inversion mode
Reverse display ON/OFF	0	0	1	0	1	0	0	1	1	REV	REV=0: normal display REV=1: reverse display
Entire display ON/OFF	0	0	1	0	1	0	0	1	0	EON	EON=0: normal display EON=1: entire display ON

Instruction	A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description
Power control	0	0	0	0	1	0	1	VC	VR	VF	Control power circuit operation
Select DC-DC step-up	0	0	0	1	1	0	0	1	DC1	DC0	Select the step-up of internal voltage converter
Select regulator register	0	0	0	0	1	0	0	R2	R1	R0	Select the internal resistance ratio of the regulator resistor
Select electronic volume register	0	0	1	0	0	0	0	0	0	1	2-byte instruction to specify the reference voltage
	0	0	x'	x'	EV5	EV4	EV3	EV2	EV1	EV0	
Select LCD bias	0	0	0	1	0	1	0	B2	B1	B0	Select LCD bias
Bias Power Save	0	0	1	1	1	1	0	0	1	1	Bias Power save
	0	0	0	0	0	0	0	0	0	0	Save the Bias current consumption
SHL select	0	0	1	1	0	0	SHL	x'	x'	x'	COM bi-directional selection SHL=0: normal direction SHL=1: reverse direction
ADC select	0	0	1	0	1	0	0	0	0	ADC	SEG bi-direction selection ADC=0: normal direction ADC=1: reverse direction
Oscillator on start	0	0	1	0	1	0	1	0	1	1	Start the built-in oscillator
Set power save mode	0	0	1	0	1	0	1	0	0	P	P=0: normal mode P=1: sleep mode
Release power save mode	0	0	1	1	1	0	0	0	0	1	release power save mode
Reset	0	0	1	1	1	0	0	0	1	0	initial the internal function
Set data direction & display data length(DDL)	x'	x'	1	1	1	0	1	0	0	0	2-byte instruction to specify the number of data bytes. (SPI mode)
	x'	x'	D7	D6	D5	D4	D3	D2	D1	D0	
Select FRC and PWM mode	0	0	1	0	0	1	0	FRC	PWM1	PWM0	FRC(1:3FRC, 0:4FRC) PWM1 PWM0 0 0 9PWM 0 1 9PWM 1 0 12PWM 1 1 15PWM
NOP	0	0	1	1	1	0	0	0	1	1	<u>No operation</u>
Test Instruction	0	0	1	1	1	1	x'	x'	x'	x'	<u>Don't use this instruction</u>

Instruction	A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description
Set white mode and 1 st /2 nd frame, set pulse width	0	0	1	0	0	0	1	0	0	0	Set white mode and 1 st /2 nd frame
Set white mode and 3 rd /4 th frame, set pulse width	0	0	WB3	WB2	WB1	WB0	WA3	WA2	WA1	WA0	Set white mode and 3 rd /4 th frame
Set light gray mode and 1 st /2 nd frame, set pulse width	0	0	1	0	0	0	1	0	1	0	Set light gray mode and 1 st /2 nd frame
Set light gray mode and 3 rd /4 th frame, set pulse width	0	0	LD3	LD2	LD1	LD0	LC3	LC2	LC1	LC0	Set light gray mode and 3 rd /4 th frame
Set dark gray mode and 1 st /2 nd frame, set pulse width	0	0	1	0	0	0	1	1	0	0	Set dark gray mode and 1 st /2 nd frame
Set dark gray mode and 3 rd /4 th frame, set pulse width	0	0	DD3	DD2	DD1	DD0	DC3	DC2	DC1	DC0	Set dark gray mode and 3 rd /4 th frame
Set dark mode and 1 st /2 nd frame, set pulse width	0	0	1	0	0	0	1	1	1	0	Set dark mode and 1 st /2 nd frame
Set dark mode and 3 rd /4 th frame, set pulse width	0	0	BB3	BB2	BB1	BB0	BA3	BA2	BA1	BA0	Set white mode and 3 rd /4 th frame

指令介绍

Set Mode Register

2-byte instruction to set FR (Frame frequency control) and BE (Booster efficiency control)

The 1st Instruction

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	1	0	0	0

The 2nd Instruction

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	FR3	FR2	FR1	FR0	0	BE	x'	0

Frame frequency

This command is used to set the frame frequency.

FR ₃	FR ₂	FR ₁	FR ₀	FR frequency
0	0	0	0	77 Hz ±5%
0	0	0	1	51 Hz ±20%
0	0	1	0	55 Hz ±20%
0	0	1	1	58 Hz ±20%
0	1	0	0	63 Hz ±20%
0	1	0	1	67 Hz ±20%
0	1	1	0	68 Hz ±20%
0	1	1	1	70 Hz ±20%
1	0	0	0	73 Hz ±20%
1	0	0	1	75 Hz ±20%
1	0	1	0	80 Hz ±20%
1	0	1	1	85 Hz ±20%
1	1	0	0	91 Hz ±20%
1	1	0	1	102 Hz ±20%
1	1	1	0	113 Hz ±20%
1	1	1	1	123 Hz ±20%

Booster Efficiency

The ST7541 incorporates software configurable Booster Efficiency Command. It could be used with Voltage multiplier to get the suitable Vout and Power consumption. Default setting is Level 2.

Flag	Description	
BE	0	Booster Efficiency Level 1
	1	Booster Efficiency Level 2

Read Display Data

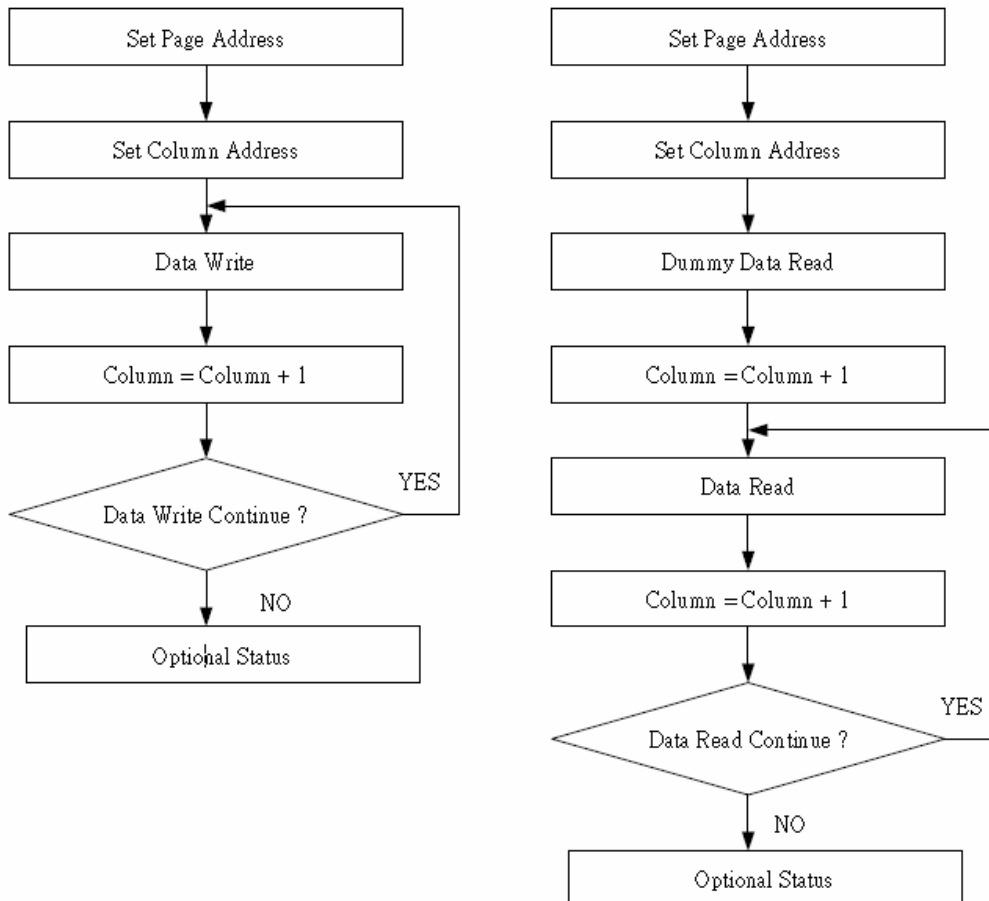
8-bit data from Display Data RAM specified by the column address and page address can be read by this instruction. As the column address is increased by 1 automatically after each this instruction, the microprocessor can continuously read data from the addressed page. A dummy read is required after loading an address into the column address register. Display Data cannot be read through the serial interface.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	Read data							

Write Display Data

8-bit data of Display Data from the microprocessor can be written to the RAM location specified by the column address and page address. The column address is increased by 1 automatically so that the microprocessor can continuously write data to the addressed page. During auto-increment, the column address wraps to 0 after the last column is written.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	Write data							



Read Status

Indicates the internal status of the ST7541

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	BUSY	ON/OFF	RES	MF2	MF1	MF0	DS1	DS0

Flag	Description
BUSY	The device is busy when internal operation or reset. Any instruction is rejected until BUSY goes Low. 0: chip is active, 1: chip is being busy
ON	Indicates display ON / OFF status 0: display OFF, 1: display ON
RESET	Indicates the initialization is in progress by RESET signal. 0: chip is active, 1: chip is being reset
MF	Manufacturer ID; recommended value: MF2 MF1 MF0 = [0 0 0] The value of MF2, MF1 and MF0 will follow the hardware selection.
DS	Display size ID; recommended value: DS1 DS0 = [1 0] The value of DS1 and DS2 will follow the hardware selection.

ICON Control Register ON/OFF

This instruction makes ICON enable or disable. By default, ICON display is disabled (ICON= 0). When ICON control register is set to "1", ICON display is enabled and page address is set to "16". Then user can write data for icons. It is impossible to set the page address to "16" by Set Page Address instruction. Therefore, when writing data for icons, ICON control register ON instruction would be used to set the page address to "16". When ICON control register is set to "0", ICON display is disabled.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	0	1	ICON

ICON=0: ICON disable (default)

ICON=1: ICON enable & set the page address to 16

Set Page Address

Sets the Page Address of display data RAM from the microprocessor into the page address register. Any RAM data bit can be accessed when its Page Address and column address are specified. Along with the column address, the Page Address defines the address of the display RAM to write or read display data. Changing the Page Address doesn't affect the display status. Set Page Address instruction can not be used to set the page address to "16". Use ICON control register ON/OFF instruction to set the page address to "16".

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	1	P3	P2	P1	P0

P3	P2	P1	P0	Page
0	0	0	0	0
0	0	0	1	1
:	:	:	:	:
1	1	1	0	14
1	1	1	1	15

Set Column Address

Sets the Column Address of display RAM from the microprocessor into the column address register. Along with the Column Address, the Column Address defines the address of the display RAM to write or read display data.

When the microprocessor reads or writes display data to or from display RAM, Column Addresses are automatically increased.

Set Column Address MSB

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	0	Y7	Y6	Y5

Set Column Address LSB

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	Y4	Y3	Y2	Y1

Y8	Y7	Y6	Y5	Y4	Y3	Y2	Column address [Y7:Y1]
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
:	:	:	:	:	:	:	:
1	1	1	1	1	1	0	126
1	1	1	1	1	1	1	127

Set Modify-Read

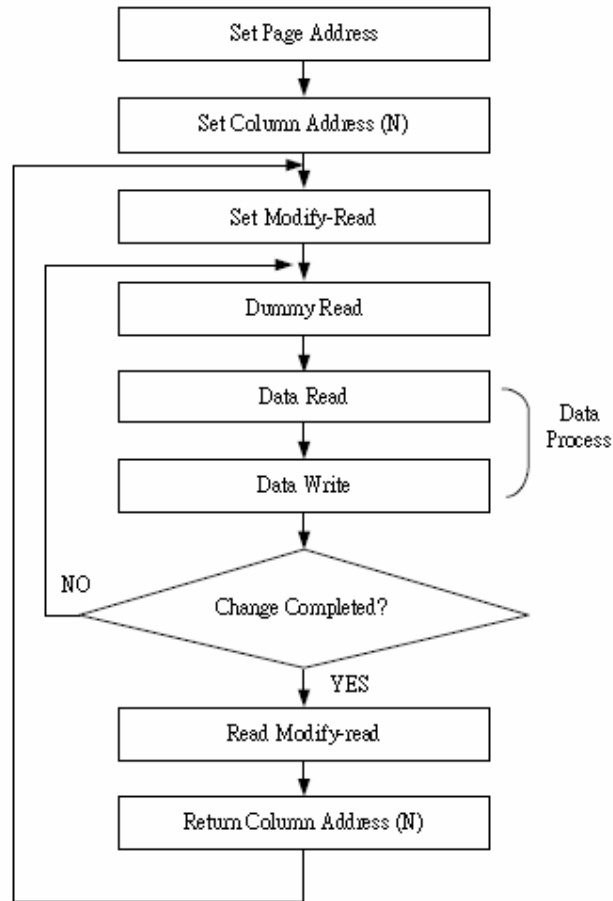
This instruction stops the automatic increment of the column address by the read display data instruction, but the column address is still increased by the write display data instruction. And it reduces the load of microprocessor when the data of a specific area is repeatedly changed during cursor blinking or others. This mode is canceled by the reset Modify-Read instruction.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	0	0

Reset Modify-Read

This instruction cancels the Modify-Read mode, and makes the column address return to its initial value just before the set Modify-Read instruction is started.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	1	1	1	0



Display ON / OFF

Turns the display ON or OFF.

This command has priority over Entire Display On/Off and Reverse Display On/Off. Commands are accepted while the display is off, but the visual state of the display does not change.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	1	1	DON

DON = 1: display ON

DON = 0: display OFF

Set Initial Display Line Register

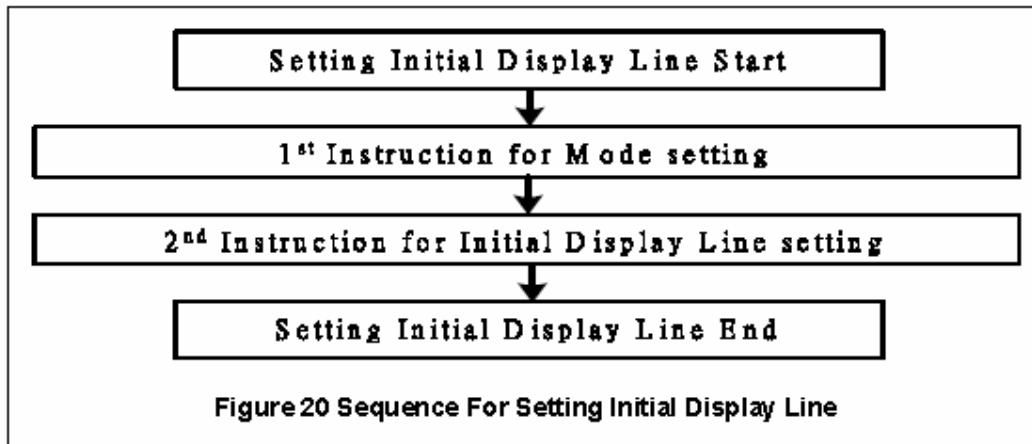
Sets the line address of display RAM to determine the initial display line using 2-byte instruction. The RAM display data is displayed at the top of row(COM0) of LCD panel.

The 1st Instruction

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	0	0	0	x	x

The 2nd Instruction

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	x	S6	S5	S4	S3	S2	S1	S0
S6	S5	S4	S3	S2	S1	S0	Line address		
0	0	0	0	0	0	0	0		
0	0	0	0	0	0	1	1		
0	0	0	0	0	1	0	2		
0	0	0	0	0	1	1	3		
:	:	:	:	:	:	:	:		
1	1	1	1	1	0	0	124		
1	1	1	1	1	0	1	125		
1	1	1	1	1	1	0	126		
1	1	1	1	1	1	1	127		

**Set Initial COM0 Register**

Sets the initial row (COM) of the LCD panel using the 2-byte instruction. By using this instruction, it is possible to realize the window moving without the change of display data.

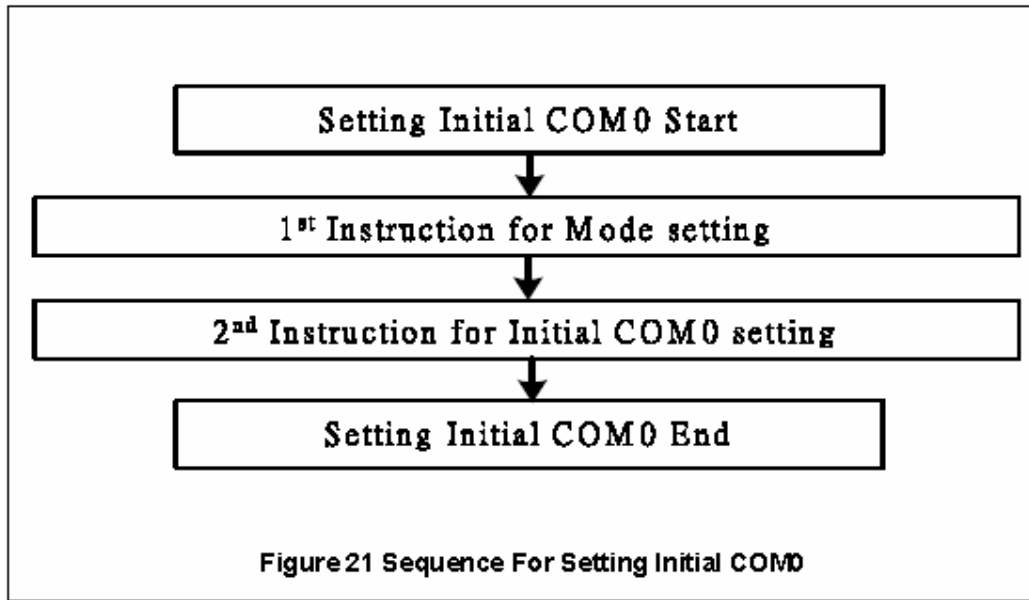
The 1st Instruction

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	0	0	1	x	x

The 2nd Instruction

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	x	C6	C5	C4	C3	C2	C1	C0

C6	C5	C4	C3	C2	C1	C0	Initial COM0
0	0	0	0	0	0	0	COM0
0	0	0	0	0	0	1	COM1
0	0	0	0	0	1	0	COM2
0	0	0	0	0	1	1	COM3
:	:	:	:	:	:	:	:
1	1	1	1	1	0	0	COM124
1	1	1	1	1	0	1	COM125
1	1	1	1	1	1	0	COM126
1	1	1	1	1	1	1	COM127



Set Partial Display Duty Ratio

Sets the duty ratio within range of 16 to 128 (ICON disabled) or 17 to 129 (ICON enabled) to realize partial display by using the 2-byte instruction.

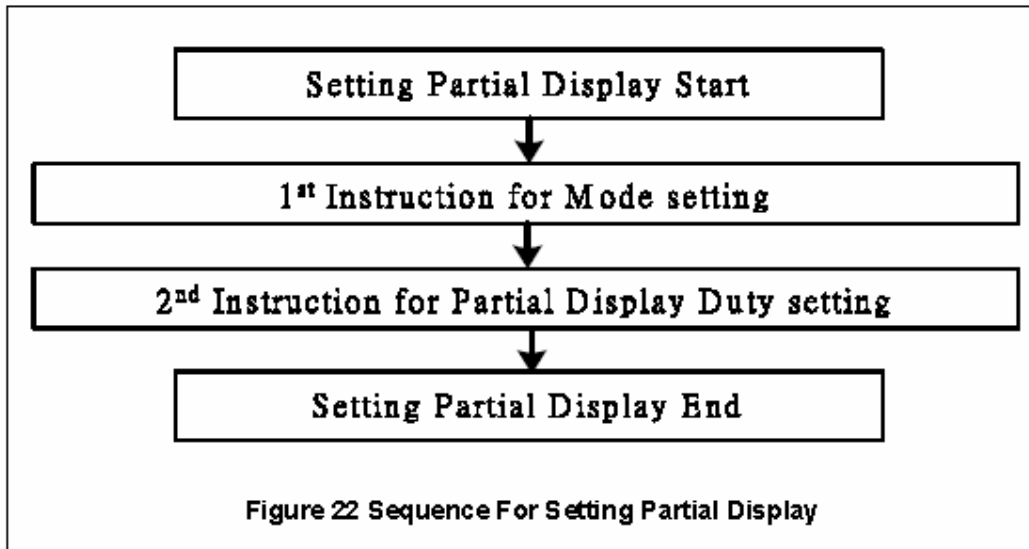
The 1st Instruction

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	0	1	0	x	x

The 2nd Instruction

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	D7	D6	D5	D4	D3	D2	D1	D0

D7	D6	D5	D4	D3	D2	D1	D0	Selected partial duty ratio (ICON disabled)	Selected partial duty ratio (ICON enabled)
0	0	0	0	0	0	0	0	No operation	No operation
:	:	:	:	:	:	:	:		
0	0	0	0	1	1	1	1		
0	0	0	1	0	0	0	0	1/16	1/17
0	0	0	1	0	0	0	1	1/17	1/18
:	:	:	:	:	:	:	:	:	:
0	1	1	0	0	1	0	0	1/100	1/101
:	:	:	:	:	:	:	:	:	:
0	1	1	1	1	1	1	1	1/127	1/128
1	0	0	0	0	0	0	0	1/128	1/129
1	0	0	0	0	0	0	1	No Operation	No Operation
:	:	:	:	:	:	:	:		
1	1	1	1	1	1	1	1		



Set N-line Inversion Register

Sets the inverted line number within range of 3 to 33 to improve the display quality by controlling the phase of the internal LCD AC signal (M) by using the 2-byte instruction.

The DC-bias problem could be occurred if K is even number. So, we recommend customers to set K to be odd number. K : D/N

D: The number of display duty ratio (D is selectable by customers)

N: N for N-line inversion (N is selectable by customers).

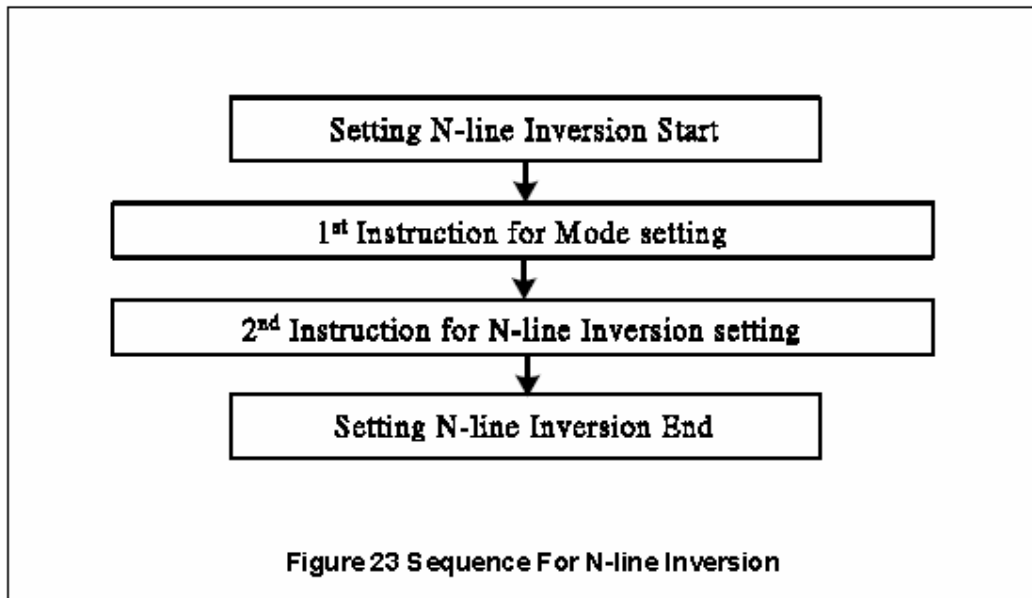
The 1st Instruction

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	0	1	1	x	x

The 2nd Instruction

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	x	x	x	0	0	0	0	0

N4	N3	N2	N1	N0	Selected n-line inversion
0	0	0	0	0	0-line inversion (frame inversion)
0	0	0	0	1	3-line inversion
0	0	0	1	0	4-line inversion
0	0	0	1	1	5-line inversion
:	:	:	:	:	:
1	1	1	0	1	31-line inversion
1	1	1	1	0	32-line inversion
1	1	1	1	1	33-line inversion

**Release N-line Inversion**

Returns to the frame inversion condition from the n-line inversion condition.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	1	0	0

Reverse Display ON / OFF

Reverses the display status on LCD panel without rewriting the contents of the display data RAM.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	1	1	REV

REV	DDRAM data = "00" – White	DDRAM data = "01" – Light gray	DDRAM data = "10" – Dark gray	DDRAM data = "11" – Dark
0 (normal)	White ("00")	Light gray ("01")	Dark gray ("10")	Dark ("11")
1 (reverse)	Dark ("11")	Dark gray ("10")	Light gray ("01")	White ("00")

Entire Display ON / OFF

Forces the whole LCD points to be turned on regardless of the contents of the display data RAM. At this time, the contents of the display data RAM are held. This instruction has priority over the Reverse Display ON / OFF instruction.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	1	0	EON

Entire	DDRAM data = "00" – White	DDRAM data = "01" – Light gray	DDRAM data = "10" – Dark gray	DDRAM data = "11" – Dark
0 (normal)	White ("00")	Light gray ("01")	Dark gray ("10")	Dark ("11")
1 (Entire)	Dark ("11")	Dark gray ("11")	Light gray ("11")	White ("11")

Power Control

Selects one of eight power circuit functions by using 3-bit register. An external power supply and part of internal power supply functions can be used simultaneously.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	0	1	VC	VR	VF

VC	VR	VF	Status of internal power supply circuits
0			Internal voltage converter circuit is OFF
1			Internal voltage converter circuit is ON
	0		Internal voltage regulator circuit is OFF
	1		Internal voltage regulator circuit is ON
		0	Internal voltage follower circuit is OFF
		1	Internal voltage follower circuit is ON

Set Bias Power Save Instruction

Consist of 2-byte Instructions

The 1st Instruction

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	1	0	0	1	1

The 2nd Instruction

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	0

This command is for saving the IC current consumption by Bias Power Saving

After this Instruction is set, Bias function is also working

Select DC-DC Step-up

Selects one of 4 DC-DC step-up to reduce the power consumption by this instruction. It is very useful to realize the partial display function.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	1	0	0	1	DC1	DC0

DC1	DC0	Selected DC-DC converter circuit
0	0	3 times boosting circuit
0	1	4 times boosting circuit
1	0	5 times boosting circuit
1	1	6 times boosting circuit

Select Regulator Resistor

Selects resistance ratio of the internal resistor used in the internal voltage regulator. See voltage regulator section in power supply circuit.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	0	0	R2	R1	R0

R2	R1	R0	1+ (Rb / Ra)
0	0	0	2.3
0	0	1	3.0
0	1	0	3.7
0	1	1	4.4
1	0	0	5.1
1	0	1	5.8
1	1	0	6.5
1	1	1	7.2

Set Electronic Volume Register

Consist of 2-byte Instructions

The 1st instruction set Reference Voltage mode, the 2nd one updates the contents of reference voltage register.

After second instruction, Reference Voltage mode is released.

The 1st Instruction: Set Reference Voltage Select Mode

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	0	0	0	0	1

The 2nd Instruction: Set Reference Voltage Register

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	x	x	EV5	EV4	EV3	EV2	EV1	EV0

EV5	EV4	EV3	EV2	EV1	EV0	Reference voltage parameter (a)
0	0	0	0	0	0	0
0	0	0	0	0	1	1
:	:	:	:	:	:	:
:	:	:	:	:	:	:
1	1	1	1	1	0	62
1	1	1	1	1	1	63

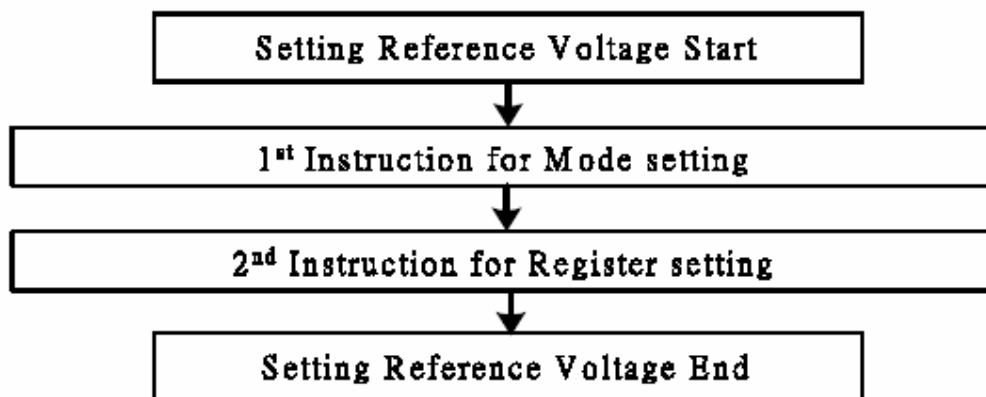


Figure 24 Sequence For Setting the Electronic Volume

Select LCD Bias

Selects LCD bias ratio of the voltage required for driving the LCD.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	1	0	B2	B1	B0

B2	B1	B0	LCD bias
0	0	0	1/5
0	0	1	1/6
0	1	0	1/7
0	1	1	1/8
1	0	0	1/9
1	0	1	1/10
1	1	0	1/11
1	1	1	1/12

SHL Select

COM output scanning direction is selected by this instruction which determines the LCD driver output status.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	0	0	SHL	x	x	x

SHL = 0: normal direction (COM0 → COM127)

SHL = 1: reverse direction (COM127 → COM0)

SHL = 0: normal direction (COM0 → COM127)

SHL = 1: reverse direction (COM127 → COM0)

ADC Select

Changes the relationship between RAM column address and segment driver. The direction of segment driver output pins could be reversed by software. This makes IC layout flexible in LCD module assembly.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	0	0	ADC

ADC = 0: normal direction (SEG0 → SEG127)

ADC = 1: reverse direction (SEG127 → SEG0)

Oscillator ON Start

This instruction enables the built-in oscillator circuit.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	0	1	1

Power Save

The ST7541 enters the Power Save status to reduce the power consumption to the static power consumption value and returns to the normal operation status by the following instructions.

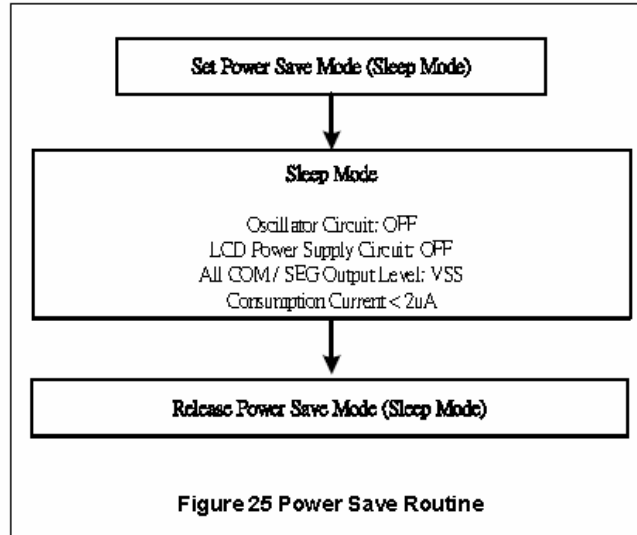
Set Power Save Mode

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	0	0	P

P = 0: normal mode, P = 1: sleep mode

Release Power Save Mode

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	0	1

**Reset**

This instruction Resets initial display line, column address, page address, and common output status select to their initial status, but does not affect the contents of display data RAM. This instruction cannot initialize the LCD power supply, which is initialized by the RESETB pin.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	1	0

Set Data Direction & Display Data Length (3-Line SPI Mode)

Consists of 2 bytes instruction.

This command is used in 3-Line SPI mode only (PS0 = "L" and PS1 = "L"). It will be two continuous commands, the first byte control the data direction (write mode only) and inform the LCD driver the second byte will be number of data bytes will be write. When A0 is not used, the Display Data Length instruction is used to indicate that a specified number of display data bytes are to be transmitted. The next byte after the display data string is handled as command data.

The 1st Instruction: Set Data Direction (Only Write Mode)

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
x	x	1	1	1	0	1	0	0	0

The 2nd Instruction: Set Display Data Length (DDL) Register

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
x	x	D7	D6	D5	D4	D3	D2	D1	D0

D7	D6	D5	D4	D3	D2	D1	D0	Display Data Length
0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	1	2
0	0	0	0	0	0	1	0	3
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	0	1	254
1	1	1	1	1	1	1	0	255
1	1	1	1	1	1	1	1	256

NOP

No operation

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	1	1

Test Instruction

This instruction is for testing IC. Please do not use it.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	1	x	x	x	x

Set PWM & FRC mode

Selects 3/4 FRC and 9 / 12 / 15 PWM

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	1	0	FRC	PWM1	PWM0

FRC	PWM1	PWM0	Status of PWM & FRC
0			4FRC
1			3FRC
	0	0	9PWM
	0	1	9PWM
	1	0	12PWM
	1	1	15PWM

Set Gray Scale Mode & Register

Consists of 2 bytes instruction. The first byte sets grayscale mode and the second byte updates the contents of gray scale register without issuing any other instruction.

– Set Gray Scale Mode

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	0	1	GM2	GM1	GM0

GM ₂	GM ₁	GM ₀	Description
0	0	0	In case of setting whit mode and 1 st / 2 nd frame
0	0	1	In case of setting whit mode and 3 rd / 4 th frame
0	1	0	In case of setting light gray mode and 1 st / 2 nd frame
0	1	1	In case of setting light gray mode and 3 rd / 4 th frame
1	0	0	In case of setting dark gray mode and 1 st / 2 nd frame
1	0	1	In case of setting dark gray mode and 3 rd / 4 th frame
1	1	0	In case of setting dark mode and 1 st / 2 nd frame
1	1	1	In case of setting dark mode and 3 rd / 4 th frame

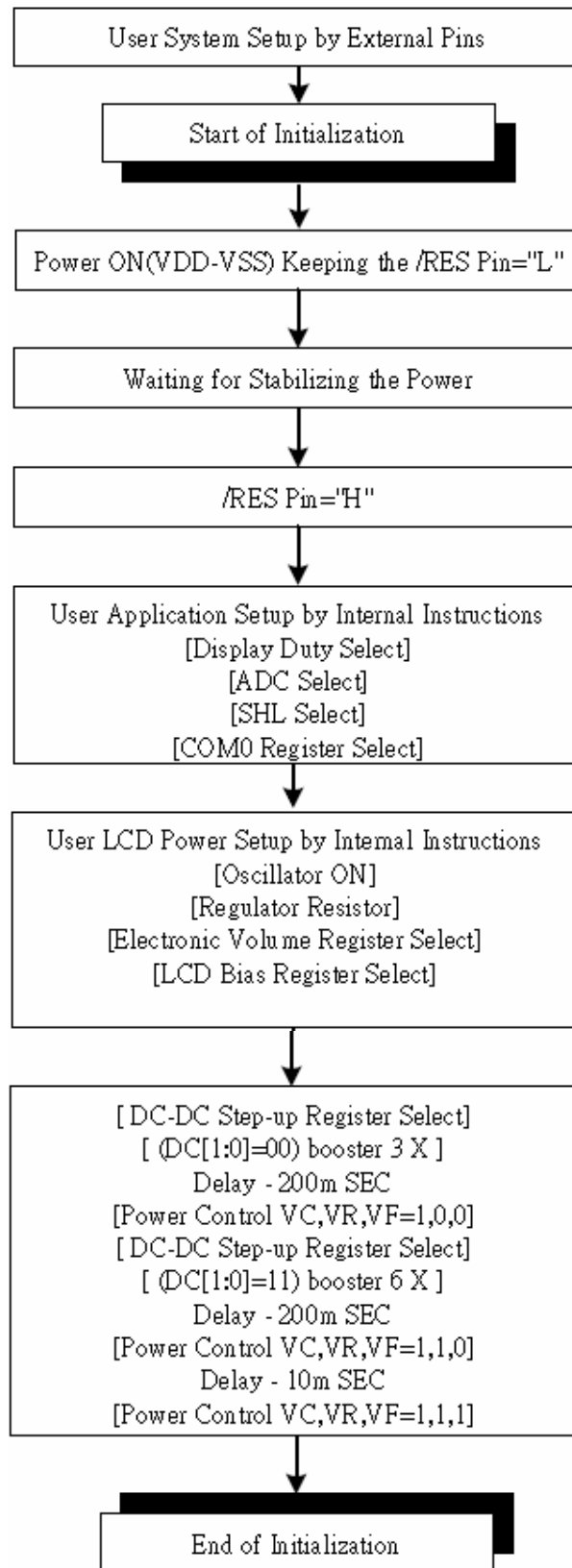
--Set Gray Scale Register

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	GB3	GB2	GB1	GB0	GA3	GA2	GA1	GA0
0	0	GD3	GD2	GD1	GD0	GC3	GC2	GC1	GC0

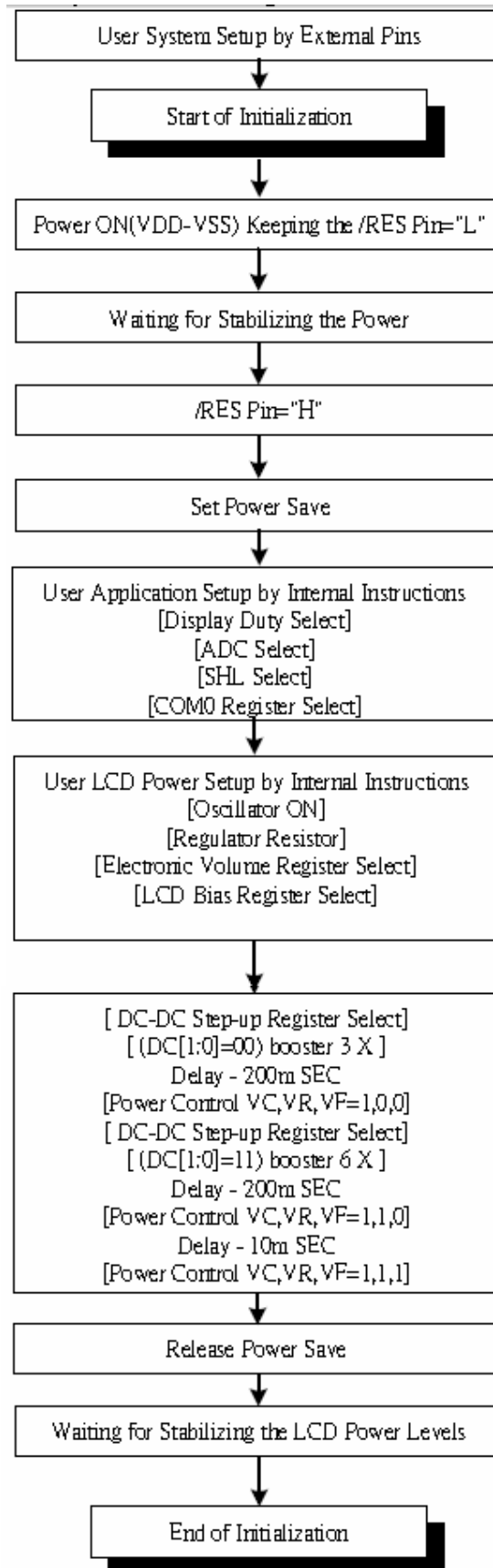
GA3, GB3, GC3, GD3	GA2, GB2, GC2, GD2	GA1, GB1, GC1, GD1	GA0, GB0, GC0, GD0	Pulse width (9 PWM)	Pulse width (12 PWM)	Pulse width (15 PWM)
0	0	0	0	0/9	0/12	0/15
0	0	0	1	1/9	1/12	1/15
:	:	:	:	:	:	:
1	0	0	1	9/9	9/12	9/15
1	0	1	0	0/9	10/12	10/15
1	0	1	0	0/9	11/12	11/15
1	1	0	0	0/9	12/12	12/15
1	1	0	1	0/9	0/12	13/15
1	1	1	0	0/9	0/12	14/15
1	1	1	1	0/9	0/12	15/15

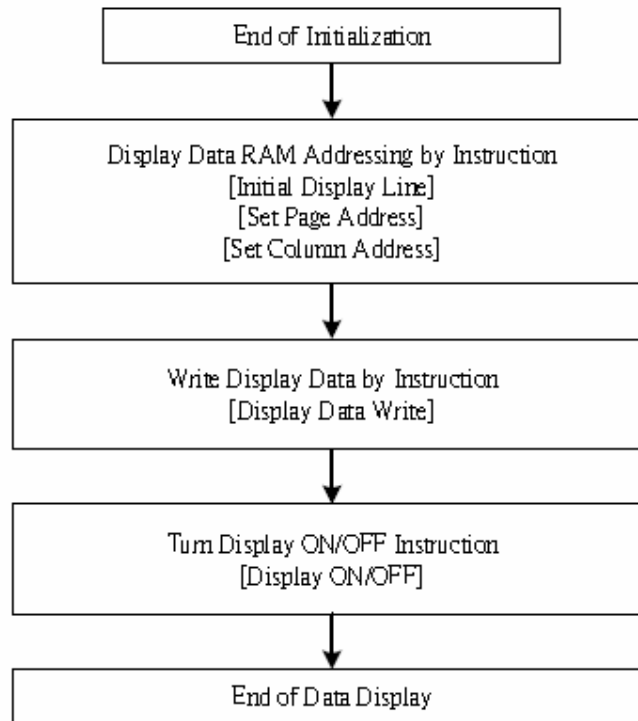
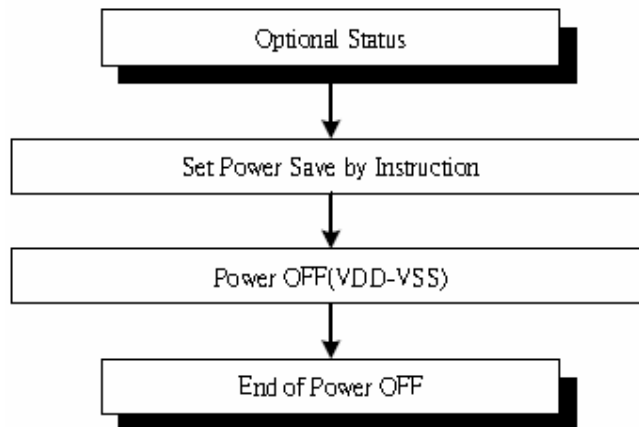
* GA3=WA3, LA3, DA3, BA3 GA2=WA2, LA2, DA2, BA2 GA1=WA1, LA1, DA1, BA1 GA0=WA0, LA0, DA0, BA0
 GB3=WB3, LB3, DB3, BB3 GA2=WB2, LB2, DB2, BB2 GA1=WB1, LB1, DB1, BB1 GA0=WB0, LB0, DB0, BB0
 GC3=WC3, LC3, DC3, BC3 GA2=WC2, LC2, DC2, BC2 GA1=WC1, LC1, DC1, BC1 GA0=WC0, LC0, DC0, BC0
 GD3=WD3, LD3, DD3, BD3 GA2=WD2, LD2, DD2, BD2 GA1=WD1, LD1, DD1, BD1 GA0=WD0, LD0, DD0, BD0

COMMAND DESCRIPTION**Referential Instruction Setup Flow: Initializing with the built-in Power Supply Circuits**



Referential Instruction Setup Flow: Initializing without the built-in Power Supply Circuits



Referential Instruction Setup Flow: Data Displaying**Referential Instruction Setup Flow: Power OFF**

11、附录

初始化程序参考:

//忙检测

```
void check_busy(void)
{
    uchar read_data=0xff;
    data_bus=0xff;
    lcd_rs=0;
    lcd_rw=1;           //读命令
    lcd_csb=0;          //片使能
    while((read_data&0x80)==0x80)
    {
        lcd_e=1;
        _nop_();
        _nop_();
        read_data=data_bus;
        lcd_e=0;
    }
    lcd_e=0;
    lcd_csb=1;          //片禁能
}
```

//写命令到寄存器

```
void send_cmd(uchar cmd) small
{
    check_busy();
    lcd_rs=0;
    lcd_rw=0;           //写命令
    lcd_csb=0;          //片使能
    data_bus=cmd;
    lcd_e=1;
    _nop_();
    _nop_();
    lcd_e=0;
    _nop_();
    _nop_();
    lcd_csb=1;          //片禁能
}
```

//写数据到 DDRAM

```
void send_dat(uchar dat) small
{
    check_busy();
    lcd_rs=1;
    lcd_rw=0;           //写数据
    lcd_csb=0;          //片使能
    data_bus=dat;
    lcd_e=1;
    _nop_();
    _nop_();
    lcd_e=0;
    _nop_();
    _nop_();
    lcd_csb=1;          //片禁能
}
```

```
//初始化
void lcd_initial(void) small
{
    lcd_rst=1;
    lcd_ps1=1;      //选择 6800 模式
    delay_nms(50);
    send_cmd(0x48); //Set partial display duty ration
    send_cmd(0x80);
    send_cmd(0xc8); //SHL select db3
    send_cmd(0xa0); //ADC select db0
    send_cmd(0x40); //Set initial display line register
    send_cmd(0x00);
    send_cmd(0x44); //Set initial com0 register
    send_cmd(0x00);
    send_cmd(0xab); //Oscillator on start
    send_cmd(0x67); //Set DC-DC 5X
    send_cmd(0x27); //Set regulator register
    send_cmd(0x81); //Set electronic volume register
    send_cmd(0x23);

    send_cmd(0x57); // bias set 1/12
    send_cmd(0x97); // set FRC and PWM

    send_cmd(0x88); // white
    send_cmd(0x00);
    send_cmd(0x89);
    send_cmd(0x00);

    send_cmd(0x8a); // light gray
    send_cmd(0x66);
    send_cmd(0x8b);
    send_cmd(0x66);

    send_cmd(0x8c); // dark gray
    send_cmd(0xaa);
    send_cmd(0x8d);
    send_cmd(0xaa);

    send_cmd(0x8e); // dark
    send_cmd(0xff);
    send_cmd(0x8f);
    send_cmd(0xff);

    send_cmd(0x2f); //power control
    send_cmd(0xaf); //display on
}
```

